AMENDMENTS TO THE SPECIFICATION

Please replace paragraph 33 starting on page 13, line 10, with the following amended paragraph:

[0033] FIG. 7 shows a system 700 that incorporates the invention. System 700 includes a plurality of DRAM chips 702, a processor 704, a memory controller 706, input devices 708, output devices 710, and optional storage devices 712. DRAM chips 702 include an array of memory cells. One or more DRAM chips 702 also include one or more circuits of the invention to ~~generates~~ generate multi-phase clock signals using hierarchical delays. The circuits of the invention may, for example, be used to synchronize data output by the DRAMs with an external clock signal (e.g., synchronous DRAM (SDRAM)). Data and control signals are transferred between processor 704 and memory controller 706 via bus 714. Similarly, data and control signals are transferred between memory controller 706 and DRAM chips 702 via bus 716. Input devices 708 can include, for example, a keyboard, a mouse, a touch-pad display screen, or any other appropriate device that allows a user to enter information into system 700. Output devices 710 can include, for example, a video display unit, a printer, or any other appropriate device capable of providing output data to a user. Note that input devices 708 and output devices 710 can alternatively be a single input/output device. Storage devices 712 can include, for example, one or more disk or tape drives.